REMARKS

Claims 1 and 16 have been amended. No claims have been canceled. No new claims have been added. Claims 1-16 are pending.

Claims 4-15 stand objected to. The Office Action alleges the use of the label "second" results in a lack of antecedent basis if there is no corresponding "first" label. Similarly, the Office Action further alleges the use of the label "third" results in a lack of antecedent basis if there are no corresponding "first" and "second" labels. This objection is respectfully traversed.

Independent claim 1, recites a power supply apparatus which comprise a first power supply circuit and a second power supply circuit. The claims which depend from claim 1 recite further details regarding power supply apparatus. For example, claim 3 depends from claim 1 and recites that the first power supply circuit is comprised of a "first" reference voltage generator and a "first" voltage divider. Similarly, claim 4 depends from claim 1 and recites that the second power supply circuit is comprised of a "second" reference voltage generator and a "second" voltage divider. Claim 5 depends from claim 1 and further recites that the second power supply circuit includes a series regulator which comprises a "third" reference voltage generator and a "third" voltage divider.

As used above, the terms "first," "second," and "third" are used as labels, not as counting elements. As such, there is no issues regarding antecedent basis. Accordingly, the objection to claims 4-15 should be withdrawn.

Claims 1, 3, 5, and 16 stand rejected under 35 U.S.C. 102(b) as being anticipated by Manabe (U.S. Patent No. 6,236,194). Claims 1-2 and 16 stand rejected under 35 U.S.C. 102(b) as being anticipated by Geyer (U.S. Patent No. 6,249,110).

Claims 1 and 16 stand rejected under 35 U.S.C. 102(b) as being anticipated by Hirake (U.S. Publication 2002-0041178). Claim 4 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Hirake in view of Geyer. Claims 6-7 and 8-9 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Geyer in view of Hirake. Claims 10-11 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Geyer in view of Manabe. Claims 12-15 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Geyer in view of Manabe and Hirake. These rejections are respectfully traversed.

Claim 1 recites, *inter alia,* "a first power supply circuit that converts a source voltage ... into a first voltage and providing the first voltage to an output voltage terminal; and a second power supply circuit that converts the source voltage from ... into a second voltage and provides the second voltage to the output terminal, said second power supply circuit being controlled to be turned on and off; ... wherein said first and second voltages are unequal."

Claim 16 recites, *inter alia,* "A ... method for supplying an output voltage, comprising: in response to voltage at an output voltage terminal, converting the source voltage into a first voltage and providing the first voltage to the output terminal; and in response to a control signal, converting the source voltage into a second voltage and providing the second voltage to the output terminal; ... wherein said first and second output voltages are unequal."

Manabe discloses at Fig. 2 a constant voltage power supply 21. The constant voltage power supply comprises a high speed voltage stabilizing part 29a having large current consumption by superior load transient response (column 5, lines 14-19) and a low speed voltage stabilizing part 29b having reduced current consumption (column 5, lines 54-67). The high 29a and low 29b speed voltage stabilizing parts are identical except for transistor sizing. Column 5, lines 54-56 and lines 19-26. Both parts 29a and

29b receiving input power Vbat from a power input node 23 and both drive the gate of a output transistor 25, which is series coupled by its source and drain between the input power node 23 and an output power node 27. The output power node 27 supplies an output power at voltage Vout to a load 3. A switching circuit couples the output of only one of parts 29a and 29b to the gate of the output transistor 25 based on the characteristics of the load 3. Column 6, lines 27-58. Significantly, neither parts 29a or 29b are coupled to "an output voltage terminal that provides an output voltage," as both parts are coupled to control the output transistor 25. Manabe therefore fails to disclose or suggest the above quoted portions of claims 1 and 16.

Geyer discloses at Fig. 1 a power supply circuit which accepts input voltage UB at input node A1 and which delivers output voltage UA at output node A2. Coupled in parallel between nodes A1 and A2 are power circuits LR and SR. Power circuit LR includes a in-phase regulator, while power circuit SR includes a switched mode regulator. Geyer's power supplied works as follows. When the input voltage UB is greater than 8 volts, power circuit LR is turned off (column 3, lines 11-22), power supply circuit SR is turned on and is solely responsible for the output voltage UA at node A2 (column 3, lines 1-4). When the input voltage UB is below 8 volts, power circuit SR cannot operate correctly and is shut down. Column 3, lines 4-6. When the input voltage UB is between 6 volt and 8 volt, power circuit LR supplies the output voltage UA at the output node A2. Geyer therefore discloses a power supply circuit in which only a first circuit (LR) supplies the output power when the input power is at a first voltage range (6-8 volts), and in which only a second circuit (SR) supplies the output power when the input power is at a second voltage range (8+ volts). Significantly, since both the first (LR) and second (SR) circuits are directly coupled to the output node A2, and only one of the two circuits operates at any given time, both

circuits produce the same output voltage UA. Geyer therefore fails to disclose or suggest the above quoted portions of claims 1 and 16.

Hiraki discloses at Fig. 1 a power supply circuit, including a first power circuit including an internal reference voltage generator circuit 111, a series regulator 130 and a second power circuit including a switching regulator 120. The internal reference voltage generator circuit 111 generates a reference voltage which is supplied both power circuits 130, 120. Both power circuits 130, 120 provide an output voltage to a common output node to provide the Vddi voltage for the load (e.g., CPU 101). Significantly, the output voltages of the two power circuits 130, 120 are equal to the reference voltage Vref. Pages 2-3, paragraph [0033]. Hiraki therefore fails to disclose or suggest the above quoted portions of claims 1 and 16.

Claims 1 and 16 are believed to be allowable over the prior art of record. Dependent claims 2-15 are also believed to be allowable for at least the same reasons as the independent claims.

In view of the above amendment, applicant believes the pending application is in condition for allowance.

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Respectfully submitted,

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